REMARKS

Claims 1-22 are pending in the application. Claims 2, 8, 12, and 19 have been amended, leaving claims 1-22 for consideration upon entry of the present Amendment. Applicant has amended the specification to describe what is already illustrated in Figures 5B and 6 and what is already described in the Summary of the Invention. Accordingly, no new matter has been entered. Applicant respectfully requests reconsideration in view of the following amendment and remarks.

Claims 1-22 stand rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter that was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Applicant respectfully traverses.

MPEP 2163.03 states: "While a question as to whether a specification provides an adequate written description may arise in the context of an original claim which is not described sufficiently * * *, there is a strong presumption that an adequate written description of the claimed invention is present in the specification as filed. * * * Consequently, rejection of an original claim for lack of written description should be rare." In this case, the specification, along with the drawings, does provide an adequate written description for the claims.

The inquiry into whether the description requirement is met must be determined on a case-by-case basis and is a question of fact. MPEP 2163.04. In this case, the Summary of the Invention section of the specification clearly supports the claims. See page 6, line 10 to page 9, line 16. On this basis alone, the Examiner should withdraw the rejection.

In addition, there is further support for the claims in the specification. For instance, claims 2, 8-14, and 19-22 require a first thin film transistor having a first conductive region formed of a semiconductor film and connected to a data line. Upon review of Figures 3 and 6 and the supporting description in the specification, page 15, lines 3-6 state the following: "A contact hole is formed at predetermined position of the interlayer insulating film 14, and respective semiconductor layers are exposed at the bottom of a contact hole C1 for the data line DL and the active layer of the first TFT 1." Thus, it is clear from Figure 6 and this description that a first conductive region is the area

in which the data line DL intersects with semiconductor film, which is also the active layer 12 (see page 12, line 25 – page 13, line 8). The fact that Applicant has not specifically called out that area as first conductive region on Figure 6 does not mean that the specification does not support the claim. The figures and the written description fully support this limitation.

Claims 2, 8-14, and 19-22 also require that the first thin film transistor has a second conductive region and that a second gate electrode connected to the second conductive region. In Figures 3, 4, 5A, and 7, the gate electrode 15 of the second thin film transistor 4 is connected to the second capacitor electrode 3 via contact holes C5, C4, and wiring 30. As with the first conductive region, the second conductive region of the first thin film transistor 1 is formed in the active layer 12. Thus, it is clear from the figures that a second conductor region of the first thin film transistor is the same region as the source region, designated by S on Figure 3.

In addition, claims 2, 8-14, and 19-22 also require a second thin film transistor having a third conductive region formed of a semiconductor film and connected to a power source line of said EL element. This limitation is support by Figures 3 and 5B and the supporting description in the specification. As explained above, the semiconductor film is the active layer 16 (see page 12, line 25 – page 13, line 8). In addition, the specification describes that the semiconductor layer is exposed at the bottom of the contact hole C2 for the power source line VL and the active layer of the second TFT 4. Figure 5B and this description clearly indicate that third conductive region is at the area in which the power line and the active layer intersect. In addition, it should also be noted that Applicant has labeled this conductive region as IR2 on Figure 5B.

In addition, claims 2, 8-14, and 19-22 also require a fourth conduction region connected said EL element. This limitation is support by Figures 3 and 5B and the supporting description in the specification. As explained above, the semiconductor film is the active layer 16 (see page 12, line 25 – page 13, line 8). In addition, the specification the anode 6 and the source of the second TFT 4 must be connected, and therefore a contact hole C3 is formed through the planarized film 18 and the interlayer insulating film 14. Through this contact hole C3, the second active layer 16 is connected to the transparent

electrode forming the anode 6 of the organic EL element 20. See page 16, lines 15-20. Figure 5B and this description clearly indicate that fourth conductive region is at the area in which the source electrode intersects with the active layer. In addition, it should also be noted that Applicant has labeled this conductive region as IR1 on Figure 5B.

In addition, claims 1, 3-7, and 15-18 recite that a thin film transistor has a first and second conductive region and that one of the first and second conductive regions are connected to the EL element. This limitation is similar to the one described above with respect to the fourth conductive region. Thus, the discussion set forth above applies to this limitation.

The specification also provides further support as to the definition of the first conductive region, the second conductive region, the third conductive region, and the fourth conductive region. On page 6, lines 17-24, there is the following explanation: "Generation of a leak current is prominent when light enters a depletion layer formed in the vicinity of a junction interface (interface between a channel and a source or drain). While the leak current generated in the interface of one of the first and second or the third and fourth conductive regions of the TFT is controlled by the gate electrode before flowing in to the EL element, the leak current generated in the other conductive region connected to the EL element cannot be controlled and flows into the EL element." That description defines a junction interface as the interface between a channel and a source or drain. The description then goes on to discuss the leak current generated in "the interface" of conductive regions is controlled by the gate electrode.

One skilled in the art would recognize that the first and second conductive regions of the first thin film transistor and the third and fourth conductive regions of the second thin film transistor may be impurity doped source or drain regions. A conductive region may be switched from source to drain region or vice versa depending on whether the transistor is p-channel or n-channel type. Accordingly, the source region (S) and the drain region (D) shown on Figure 3 also illustrate the location the conductive regions.

In view of the foregoing, it is respectfully submitted that the instant application is in condition for allowance. Accordingly, it is respectfully requested that this application be allowed and a Notice of Allowance issued. If the Examiner believes that a telephone

conference with Applicant's attorneys would be advantageous to the disposition of this case, the Examiner is cordially requested to telephone the undersigned.

In the event the Commissioner of Patents and Trademarks deems additional fees to be due in connection with this application, Applicant's attorney hereby authorizes that such fee be charged to Deposit Account No. 06-1130.

Respectfully submitted,

CANTOR COLBURN LLP

By: Lisa Bongiovi

Lisa A. Bongiovi
Registration No. 48,933
CANTOR COLBURN LLP
55 Griffin Road South
Bloomfield, CT 06002
Telephone (860) 286-2929
Facsimile (860) 286-0115
Customer No. 23413

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